TITLE

DATA RECOVERY CIRCUIT, PHASE DETECTION CIRCUIT AND METHOD FOR DETECTING AND CORRECTING PHASE CONDITIONS

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is based upon and claims the benefit of U.S. provisional application No. 60/423,392 filed November 4, 2002, the contents of which are incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a data recovery circuit, and more particularly, to a circuit and a method for minimizing a phase error of a sampling clock in a data recovery circuit.

Description of the Related Art

DVI (Digital Visual Interface) is a digital display interface standard established by several PC and graphic card manufacturers. Thanks to the high speed and the excellent display quality of the DVI transmission system, it is foreseeable that DVI interface will become a widely used standard interface for image display in the near future.

Figure 1 illustrates the data transmission structure of a display system configured with DVI standard. The system mainly comprises a host portion 10 and a display portion 20. In the host portion 10, a graphic card 12 is used to generate three 8-bit digital image signals R[0:7], G[0:7], and B[0:7] respectively for the three primary colors of red, green and blue. According to DVI standard, these 8-bit digital image signals are then sent to a DVI encoder 14 to

be encoded into 10-bit DVI image signals R'[0:9], G'[0:9] and B'[0:9], which are subsequently converted by a DVI transmitter 16 into differential serial image signals [R+:R-], [G+:G-] and [B+:B-] and transmitted by a DVI transmission cable 18 to the display portion 20. Note that the three differential serial image signals [R+:R-], [G+:G-] and [B+:B-] should be transmitted respectively by three pairs of differential transmission lines. Moreover, these differential serial image signals should be transmitted at a frequency equal to ten times the rate of the 10-bit DVI image signals since they are generated from the 10-bit signals by a parallel-to-serial conversion. However, a differential clock signal [CK+:CK-] generated by the DVI transmitter 16 is transmitted at the original rate. For simplicity, all the differential transmission lines are represented by only one DVI transmission cable 18 in Figure 1. A DVI receiver 22 in the display portion 20 is used for receiving the differential image signals and for recovering 10-bit DVI image signals from those differential image signals. Thereafter, the recovered 10-bit DVI image signals are decoded by a DVI decoder 24 into 8-bit digital image signals for display on a display panel (not shown in the drawings).

In order to recover 10-bit DVI image signals, the DVI receiver 22 is typically provided with a data recovery circuit for obtaining recovered data signals by taking samples of the differential image signals in accordance with a sampling clock generated from the received differential clock signal. A conventional serial data sampling technique is shown in Figure 3(a), in which a clock signal 32 having a frequency equal to the rate of the incoming data 30 is generated to sample the incoming data

30. Each of the rising edges of the clock signal 32 is approximated aligned to a central portion 36 of one data bit in the incoming data 30 to ensure correct sampling of the data.

Figures 3(a) and 3(b) illustrate conventional serial data sampling scheme, in which Figure 3(a) shows the condition without clock skew and Figure 3(b) shows the condition with clock skew;

However, according to the DVI standard, the differential image signal is transmitted at an extremely high rate, for example, at several giga-hertz (GHz), and it is very difficult to generate a sampling clock with such a high frequency. Furthermore, in a data transmission high up to several giga-hertz, the transmitted signals are vulnerable to jitters and high-frequency reflective interferences, which significantly reduces the effective period for valid sampling of a data bit. As can be seen in Figure 2, due to the reflective interferences 28a, the effective sampling period of a data bit 28 is reduced from T to about T/2. Therefore, if there is a significant skew between a sampling edge 38 of the sampling clock and a central portion 36 of a data bit in the incoming data 30, i.e., the condition that the sampling clock 34 is out of phase with the incoming data 30, as shown in Figure 3(b), then it is very possible to obtain an incorrect sampling data.

Accordingly, there is a need to develop a data recovery circuit, which is suitable for applications of high frequency serial data transmission, and in which a sampling clock with lower frequency can be used for sampling the high frequency serial data while the sampling edges of the sampling clock are always maintained in positions aligned with the central portions of the data bits.

SUMMARY OF THE INVENTION

The object of the present invention is to provide a data recovery circuit having a sampling circuit that can be operated at a lower frequency. Therefore, the data recovery circuit is suitable for applications of high frequency serial data transmission.

Another object of the present invention is to provide a data recovery circuit having a phase detection and correction circuit for dynamically detecting and controlling the phase of a sampling clock signal to ensure that the sampling edges of the clock signal are always locked to the central portions of the data bits to thereby obtain correct recovered data.

In order to achieve the above objects, the data recovery circuit of the present invention comprises: a clock generator for generating a first group of sampling clock pulses and a second group of sampling clock pulses and being controlled in response to a phase control signal to adjust the phases of the first group of sampling clock pulses and the second group of sampling clock pulses; a data and phase sampling circuit for sampling approximately a central portion of each data bit in an incoming data stream in accordance with the first group of sampling clock pulses to produce a first sampled data stream while sampling approximately a transition portion between every two data bits in the incoming data stream in accordance with the second group of sampling clock pulses to produce a second sampled data stream; and a phase detection and correction circuit for determining the resemblance of each bit in the second sampled data stream to the corresponding two adjacent bits in the first sampled data stream, defining

an early condition for the phases of the sampling clocks if each bit in the second sampled data stream resembles the former of the corresponding two adjacent bits in the first sampled data stream while defining a late condition for the sampling clocks if each bit in the second sampled data stream resembles the latter of the corresponding two adjacent bits in the first sampled data stream, and producing the phase control signal on the basis of the early condition or the late condition to adjust the phases of the sampling clocks by shifting the phases backwards or forwards.

BRIEF DESCRIPTION OF THE DRAWINGS

Objects and advantages of the present invention will be fully understood from the detailed description to follow taken in conjunction with the embodiments as illustrated in the accompanying drawings, wherein:

Figure 1 illustrates the data transmission structure of a DVI display system.

Figure 2 is a diagram describing the interference to the data during high frequency transmission;

Figures 3(a) and 3(b) illustrate conventional serial data sampling scheme, in which Figure 3(a) shows the condition without a clock skew and Figure 3(b) shows the condition with a clock skew;

Figure 4 depicts a schematic block diagram of a preferred embodiment of the data recovery circuit according to the present invention;

Figure 5 is a timing diagram of the signals in the data recovery circuit according to the present invention;

Figure 6 depicts a schematic block diagram of a preferred embodiment of the phase detection and correction circuit according to the present invention;

Figure 7 depicts a circuit diagram of a preferred embodiment of the early/late determination circuit in Figure 6; and

Figure 8 depicts a circuit diagram of a preferred embodiment of the resemblance detection circuit in Figure 7.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Please refer to Figures 4 and 5, and again to Figure 1. Figure 4 shows a schematic block diagram of a preferred embodiment of the data recovery circuit 40 according to the present invention. The data recovery circuit 40 mainly comprises a clock generator 42, a data and phase sampling circuit 44 and a phase detection and correction circuit 48. In addition, the data recovery circuit 40 may further be provided with a demultiplexer 46, coupled between the data and phase sampling circuit 44 and the phase detection and correction circuit 48.

The differential clock signal [CK+:CK-] transmitted through the DVI transmission cable 18 from the host potion 10 to the display portion 20 in Figure 1 is coupled to the clock generator 42. From the received differential clock signal [CK+:CK-], the clock generator 42 generates a first group of sampling clock pulses and a second group of sampling clock pulses, each having a frequency at five times the rate of the differential clock signal [CK+:CK-]. In the preferred embodiment, the first group of sampling clock pulses includes a first clock signal CKI and a third clock signal CKIZ, and the second group of sampling clock pulses includes a second clock signal CKQ and a forth clock signal CKQZ. As previously described with reference to Figure 1, the three differential image signals [R+:R-], [G+:G-] and

[B+:B-] are transmitted at ten times of the original data rate, and thus, according to the present invention, the frequency of the first group of sampling clock pulses and the second group of sampling clock pulses used in the data recovery circuit 40 is only half of the incoming data rate. The waveforms of the four clock signals CKI, CKIZ, CKQ and CKQZ are shown in Figure 5. The first clock signal CKI and the second clock signal CKQ are substantially 90 degrees out of phase with each other. In this embodiment, the phase of the first clock signal CKI leads the phase of the second clock signal CKQ. The third clock signal CKIZ is an inverted signal of the first clock signal CKI; i.e., the phase difference between the two clock signals CKI and CKIZ is 180 degree. Similarly, there is a 180-degree phase difference between the forth clock signal CKQZ and the second clock signal CKQ. An exemplary circuit for generating two clock signals having a 90-degree phase difference is disclosed in the U.S. patent application entitled "Apparatus for generating quadrature phase signals and data recovery circuit using the same", the serial number of which has not yet been assigned, filed by the same assignee on August 26, 2003. Other schemes may also be used in generating the above described sampling clock pulses.

The four clock signals CKI、CKIZ、CKQ、CKQZ generated by the clock generator 42 are connected to the data and phase sampling circuit 44, which operates to sample a received incoming data stream In[n] 50 in accordance with the four clock signals CKI、CKIZ、CKQ、CKQZ. The incoming data stream In[n] 50 is intended to represent any one of the three differential image signals [R+:R-], [G+:G-] and [B+:B-] in Figure 1. The data and phase sampling circuit 44 is

designed to take samples of approximately the central portions 52a of the even data bits In[0], In[2], … in the incoming data stream In[n] 50 by using the rising edges of the first clock signal CKI to produce a sampled data stream D-cki as shown in Figure 5, and to take samples of approximately the central portions of the odd data bits In[1], In[3], … in the incoming data stream In[n] 50 by using the rising edges of the third clock signal CKIZ to produce a sampled data stream D-ckiz. Meanwhile, the data and phase sampling circuit 44 samples approximately the transition portions 54a between the even data bits and the odd data bits in the incoming data stream In[n] 50 by using the rising edges of the second clock signal CKQ to produce a sampled data stream Q-ckq, and samples approximately the transition portions 54b between the odd data bits and the even data bits in the incoming data stream In[n] 50 by using the rising edges of the forth clock signal CKQZ to produce a sampled data stream Q-ckqz. The sampled data stream D-cki and the sampled data stream D-ckiz are combined together to form a first sampled data stream D[n]. Similarly, the sampled data stream Q-ckq and the sampled data stream Q-ckqz are combined together to form a second sampled data stream Q[n].

Although the rising edges of the four clock signals CKI、CKIZ、CKQ、CKQZ are used in this embodiment to sample the incoming data stream In[n], it is for exemplary purpose only, not intended to limit the scope of the present invention. In another embodiment, only two clock signals CKI and CKQ that are 90 degrees out of phase with each other are used for sampling. In this case, both rising edges and falling edges of the clock signals CKI and CKQ serve as the sampling edges. Alternatively, two clock signals having the same frequency as the incoming data rate and being 180 degrees

out of phase with each other may respectively be used for sampling the central portions of the data bits and the transition portions between every two adjacent data bits. The number and the frequency of the clock signals can be chosen depending on the circuit design as long as the above described effect can be achieved.

The demultiplexer 46 connected at the output of the data and phase sampling circuit 44 is a 1:8 demultiplexer, which is used to convert the first sampled data stream D[n] and the second sampled data stream Q[n] from serial data to 8-bit parallel data, that is, to produce a first sampled data stream Dbus and a second sampled data stream Qbus. At the same time, the frequency is reduced to one-eighth the rate of the serial data stream. The first sampled data stream Dbus can be output for subsequent data recovery process. The 1:8 demultiplexer 46 in this embodiment is provided to facilitate the subsequent data recovery process and is describe for exemplary purpose only, not intended to limit the scope of the present invention. The 1:8 demultiplexer may also be replaced by a 1:4 demultiplexer, a 1:16 demultiplexer and the like. It is also possible that no demultiplexer is provided between the data and phase sampling circuit 44 and the phase detection and correction circuit 48.

The phase detection and correction circuit 48 is connected to the output of the demultiplexer 46 to receive the parallel data from the first sampled data stream Dbus and the second sampled data stream Qbus. The phase detection and correction circuit 48 determines whether a phase skew is present or absent between the incoming data stream In[n] 50 and the clock signals CKI, CKIZ, CKQ and CKQZ by processing the first sampled data stream Dbus and

the second sampled data stream Qbus. In the case that a phase skew is present, the phase detection and correction circuit 48 generates a phase control signal to the clock generator 42 to appropriately adjust the phases of the clock signals CKI, CKIZ, CKQ and CKQZ so that the sampling edges of the second clock signal CKQ and the forth clock signal CKQZ is always locked to the transition portions between two adjacent data bits. Thereby, the sampling edges of the first clock signal CKI and the third clock signal CKIZ is always locked to the central portions of the data bits to ensure the correct sampling.

The scheme for detecting phase errors by the phase detection and correction circuit 48 is described as follows. If a transition occurs at a transition portion associated with a sampling edge of the second clock signal CKQ and the forth clock signal CKQZ, i.e., in the case that one of the corresponding two adjacent data bits is "1" and the other is "0", then the probability of obtaining a sample "1" at the transition portion should be equal to the probability of obtaining a sample "0". Therefore, referring to the timing diagrams of the first sampled data stream D[n] and the second sampled data stream Q[n] in Figure 5, if the sampling edges of the second clock signal CKQ and the forth clock signal CKQZ are shifted to the left, failing to be aligned to the transition portions between two adjacent data bits, then there is a higher probability to obtain a sample value equal to the former of the two adjacent data bits. In other words, there is a higher probability that Q[0] is equal to D[0], Q[1] to D[1], Q[2] to D[2], and so on. If the sampling edges of the second clock signal CKQ and the forth clock signal CKQZ are shifted to the right, failing to be aligned to the transition portions between

two adjacent data bits, then there is a higher probability to obtain a sample value equal to the latter of the two adjacent data bits. In other word, there is a higher probability that Q[0] is equal to D[1], Q[1] to D[2], Q[2] to D[3], and so on. Therefore, by detecting the resemblance of each bit in the second sampled data stream Q[n] to the corresponding two adjacent bits in the first sampled data stream D[n], the phase detection and correction circuit 48 can determine a phase condition of the second clock signal CKQ and the forth clock signal CKQZ. The phase condition is defined as an early condition (shift-left) if each bit in the second sampled data stream Q[n] resembles the former of the corresponding two adjacent bits in the first sampled data stream D[n], while the phase condition is defined as a late condition (shift-right) if each bit in the second sampled data stream Q[n] resembles the latter of the corresponding two adjacent bits in the first sampled data stream D[n]. Based on the determination of the early condition or the late condition, the phase detection and correction circuit 48 produces the phase control signal to the clock generator 42, indicating the clock generator 42 to correct the phases of the sampling clocks CKQ and CKQZ by shifting the phases backwards (shifting to the right) or by shifting the phases forwards (shifting to the left).

Please refer to Figure 6, which depicts a schematic block diagram of a preferred embodiment of the phase detection and correction circuit according to the present invention. As shown, the phase detection and correction circuit 48 comprises an early/late determination circuit 482, an early/late summation circuit 483 and a low pass filter 489. The first sampled data stream Dbus and the second sampled data stream Qbus generated by the 1:8 demultiplexer 46 are

fed into the early/late determination circuit 482, in the format of 8-bit parallel signals, for determining whether each bit in the second sampled data stream Qbus resembles the former or the latter of the corresponding two adjacent bits in the first sampled data stream Dbus. According to the determination result, the early/late determination circuit 482 produces an early signal "Early" or a late signal "Late". The detailed structure of the early/late determination circuit 482 will be described in the following paragraph.

Please refer to Figure 7, which shows a circuit diagram of a preferred embodiment of the early/late determination circuit 482 in Figure 6. When a 8-bit parallel signal D[0:7] from the first sampled data stream Dbus and a 8-bit parallel Q[0:7] from the second sampled data stream Qbus are fed into the early/late determination circuit 482, eight data bits of the signal D[0:7] and seven data bits of the signal Q[0:6], together with the last data bits D'[7] and Q'[7] previously latched in the D-flip-flops 72a and 72b, are sent to a resemblance detection circuit 74 for performing a resemblance determination operation. A circuit diagram of a preferred embodiment of the resemblance detection circuit 74 is shown in Figure 8. The resemblance detection circuit 74 comprises eight resemblance detecting units 741~748, each of which is used for detecting two adjacent bits from the data D'[7] and D[0:7] and one corresponding bit from the data Q'[7] and Q[0:6]. Each resemblance detecting unit 741~748 detects whether or not the two adjacent bits from the data D'[7] and D[0:7] are the same (i.e., whether a transition occurs between the two data bits). Moreover, in the case that the two adjacent bits are not the same (i.e., a transition occurs), the resemblance detecting unit

741~748 detects that whether the corresponding bit from the data Q'[7] and Q[0:6] is equal to the former or the latter of the two adjacent bits from the data D'[7] and D[0:7]. If the corresponding bit from the data Q'[7] and Q[0:6] is equal to the former of the two adjacent bits from the data D'[7] and D[0:7], an resemblance signal early[n]=1 is produced at the output. On the other hand, if the corresponding bit from the data Q'[7] and Q[0:6] is equal to the latter of the two adjacent bits from the data D'[7] and D[0:7], an resemblance signal late[n]=1 is produced at the output. Taking the resemblance detecting unit 742 for example, in the case of D[0]≠D[1], which means a transition occurs between D[0] and D[1], if Q[0]=D[0], then early[1]=1 and late[1]=0; if Q[0]=D[1], then early[1]=0 and late[1]=1. In the case of D[0]=D[1], which means no transition occurs between D[0] and D[1], the resemblance condition can not be determined and thus early[1] and late[1] are both "0". The thus generated 8-bit resemblance signals early[0:7] and late[0:7] are then fed into an early/late decision circuit 75, which comprises two counters 76a and 76b respectively for counting the number of bit "1" in each of the 8-bit resemblance signals early[0:7] and late[0:7] and producing the resulting numbers N-early and N-late. The early/late decision circuit 75 further comprises a comparator circuit 78 for comparing the number N-early and the number N-late. If N-early>N-late, which means the signal Q[n] in the current group resembles the former of the corresponding two bits in the first sampled data stream, then the early/late decision circuit 75 outputs an early signal "Early=1". On the other hand, if N-early<N-late, then the early/late decision circuit 75 outputs a late signal "Late=1". If N-early=N-late, which means the phase condition of the

sampling clock cannot be determined, then the early signal "Early" and the late signal "Late" are both "0".

Referring again to Figure 6, the early signal "Early" and the late signal "Late" generated by the early/late determination circuit 482 are further fed into an early/late summation circuit 483 for performing a summation operation. The early/late summation circuit 483 includes a multiplexer 484, which operates to produce an output signal "1" when the early signal "Early" is "1" and the late signal "Late" is "0", an output signal "-1" when the early signal "Early" is "0" and the late signal "Late" is "1", and an output signal "0" when both the early signal "Early" and the late signal "Late" are "0". The early/late summation circuit 483 further includes an adder 486 and a register 488, e.g., a 20-bit register. The adder 486 performs an addition operation to add the output signal (-1, 0, 1) from the multiplexer 484 to an accumulated amount stored in the register 488, and thus produces a new accumulated amount to be stored in the register 488. The accumulated amount in the register 488 serves as an early/late summation signal. Thereby, every time the early/late summation circuit 483 receives an early signal "Early=1", the adder 486 adds one to the accumulated amount; every time the early/late summation circuit 483 receives a late signal "Late=1", the adder 486 subtracts one from the accumulated amount.

The output of the early/late summation circuit 483 is connected to the low pass filter 489. After a predetermined time interval or after the early/late summation circuit 483 performs a predetermined number of operations, the low pass filter 489 checks the polarity of the early/late summation signal. In the case that the early/late summation signal

is positive, the number of the early signals "Early" is greater than the number of the late signals "Late" and thus the sampling edges of the second clock signal CKQ and the forth clock signal CKQZ are determined to be in an early condition. Therefore, the low pass filter 489 produces a phase control signal to the clock generator 42 to correct the sampling clocks CKQ and CKQZ by appropriately shifting the phases backwards. On the other hand, in the case that the early/late summation signal is negative, the number of the late signals "Late" is greater than the number of the early signals "Early" and thus the sampling edges of the second clock signal CKQ and the forth clock signal CKQZ are determined to be in a late condition. Therefore, the low pass filter 489 produces a phase control signal to the clock generator 42 to correct the sampling clocks CKQ and CKQZ by appropriately shifting the phases forwards. In the case that the early/late summation signal is zero, no correction is made to the sampling clocks CKQ and CKQZ. Once the early/late summation signal is checked by the low pass filter 489, the register is reset to zero for the subsequent accumulation. In order to avoid deterioration of the display quality, the timing for the low pass filter 489 to check the early/late summation signal is preferably during the blank period, in which no image data is transmitted. In practice, the low pass filter 489 is designed to check the early/late summation signal and to correct the phases at a more frequent rate, for example, every 100~200 operations, before the system reaches a stable state. When the system becomes stable after a period of time, the frequency for checking the early/late summation signal can be reduced to a lower rate, for example, every 600~1000 operations.

While the present invention has been described with reference to the preferred embodiments thereof, it is to be understood that the invention should not be considered as limited thereby. Various modifications and changes could be conceived of by those skilled in the art without departuring from the scope of the present invention, which is indicated by the appended claims.